

What is claimed is:

1           1. An integrated circuit structure comprising:  
 2               a plastic substrate;  
 3               a layer of silicon dioxide or silicon nitride having a thickness such that little  
 4           or no differential strain between the substrate and said layer occurs in the normal  
 5           operating temperature range of said integrated circuit;  
 6               an antenna conductor which is bonded onto, integrated onto or printed onto  
 7           said substrate and having two conductive pads or other conductive terminal areas  
 8           where electrical connection to said antenna may be made;  
 9               an RFID tag or smart card transceiver integrated circuit integrated on said  
 10          substrate so as to have RF input/output terminals which are electrically coupled to  
 11          said terminal areas of said antenna.

1           2. An integrated circuit structure comprising:  
 2               a plastic substrate;  
 3               a layer of silicon dioxide or silicon nitride having a thickness such that little  
 4           or no differential strain between the substrate and said layer occurs in the normal  
 5           operating temperature range of said integrated circuit;  
 6               an RFID tag or smart card transceiver integrated circuit integrated on said  
 7           substrate on top of said layer of silicon dioxide or silicon nitride so as to have RF  
 8           input/output terminals, and having a layer of insulating material formed over said  
 9           integrated circuit;  
 10          an antenna conductor which is bonded onto, integrated onto or printed onto  
 11          said insulating layer covering said integrated circuit so as to make electrical  
 12          connection with said RF input/output terminals.

1           3. An integrated circuit structure comprising:  
 2               a first plastic or glass or plastic laminated to glass substrate;

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3 a layer of silicon dioxide or silicon nitride having a thickness such that little  
4 or no differential strain between the substrate and said layer occurs in the normal  
5 operating temperature range of said integrated circuit;

6 an antenna conductor which is bonded onto, integrated onto or printed onto  
7 said substrate and having two conductive pads or other conductive terminal areas  
8 where electrical connection to said antenna may be made;

9 an RFID tag or smart card transceiver integrated circuit integrated as one of a  
10 very large number of said integrated circuits on a large second plastic or glass  
11 substrate using flat panel display manufacturing equipment, said integrated circuit  
12 being cut from said second plastic or glass substrate and bonded or otherwise  
13 attached to said first plastic substrate and having RF input/output terminals; and  
14 wires connected in any way between said RF input/output terminals of said  
15 integrated circuit and said terminal areas of said antenna.

1 4. A process of making a large number of integrated circuits on a large plastic or  
2 glass or plastic laminated to glass substrate comprising:

3 selecting a plastic or glass or plastic laminated to glass substrate having a  
4 large size which is compatible with the substrate size capacity of flat panel display  
5 manufacturing machines to be used to do the subsequent deposition, photolithography,  
6 etching and laser crystallization and annealing steps necessary to form an integrated  
7 circuit thereon;

8 depositing a layer of insulating material which has a thickness and Young's  
9 Modulus which are selected in light of the thickness and Young's Modulus of said  
10 substrate so as to reduce differential strain at anticipated operating temperatures so  
11 as to eliminate or reduce reliability problems using processing steps performed at  
12 temperatures or in a manner which will not exceed the glass transition temperature  
13 of said substrate and using chemicals which will not chemically attack or otherwise  
14 damage said substrate;

15 forming an antenna with one or more terminals on said layer of insulating  
16 material using processing steps performed at temperatures or in a manner which

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17 will not exceed the glass transition temperature of said substrate and using  
18 chemicals which will not chemically attack or otherwise damage said substrate;  
19 using flat panel display manufacturing machines to deposit a layer of  
20 insulating material over said antenna and to do the insulation, metal and  
21 semiconductor deposition steps, and the photolithography, etching and pulsed laser  
22 crystallization and annealing steps necessary to form an integrated circuit of a  
23 desired functionality directly on said substrate so as to RF input/output terminals in  
24 electrical contact with said one or more antenna terminals, all said processing steps  
25 performed at temperatures or in a manner which will not exceed the glass transition  
26 temperature of said substrate and using chemicals which will not chemically attack  
27 or otherwise damage said substrate.

- 1 5. A process of making a large number of integrated circuits on a large substrate  
2 comprising:
- 3 selecting a first plastic or glass or plastic laminated to glass substrate having  
4 a large size which is compatible with the substrate size capacity of flat panel display  
5 manufacturing machines to be used to do the subsequent deposition, photolithography,  
6 etching steps needed to form an antenna or compatible with the substrate size  
7 capacity that can be processed by a silk screen printer to print an antenna;  
8 depositing a layer of insulating material which has a thickness and Young's  
9 Modulus which are selected in light of the thickness and Young's Modulus of said  
10 substrate so as to reduce differential strain at anticipated operating temperatures so  
11 as to eliminate or reduce reliability problems using a process which will not melt,  
12 warp, deform, chemically attack or otherwise damage said first substrate;  
13 using a flat panel display manufacturing machine or silk screen printer to  
14 form a plurality of antennas at a plurality of locations on said first substrate with  
15 one or more terminals on said layer of insulating material using deposition,  
16 photolithography, etching or printing processes which will not melt, warp, deform,  
17 chemically attack or otherwise damage said first substrate;  
18 dicing said first substrate up into many individual substrates, each with its  
19 own antenna formed thereon;

selecting a second plastic or glass or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form a thin film integrated circuit;

using flat panel display manufacturing machines to do the insulation, metal and semiconductor deposition steps, and the photolithography, etching and pulsed laser crystallization and annealing steps necessary to form an integrated circuit of a desired functionality on said second substrate so as to RF input/output terminals, all said processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said second substrate and using chemicals which will not chemically attack or otherwise damage said second substrate;

dicing said second substrate up into many integrated circuits and bonding or otherwise attaching each functional integrated circuit to one of said individual plastic substrates cut from said first substrate; and

wire bonding wires to connect said RF input/output terminals of said integrated circuit to said one or more terminals of said antenna on said individual first substrate.

6. A process of making a large number of integrated EEPROM cells on a large substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said EEPROM cells thereon;

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature

of said plastic substrate and using chemicals which will not chemically attack or otherwise damage said plastic substrate;

using flat panel display manufacturing machines to do the insulation, metal and semiconductor deposition steps, and the photolithography, etching and pulsed laser crystallization and annealing steps necessary to form a plurality of EEPROM memory cells directly on said plastic substrate, all said processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said plastic substrate and using chemicals which will not chemically attack or otherwise damage said plastic substrate.

7. A process for manufacturing an integrated circuit including MOS transistors and EEPROM cells on a substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition

temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silicon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silicon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses;

masking off areas of said integrated circuit where EEPROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transition temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the EEPROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a

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54 layer of intergate insulator from which will be formed the insulation layer  
55 between the floating gate and the control gate of each EEPROM cell, said  
56 deposition being accomplished by PECVD or some other process which will  
57 form an insulator of high enough quality to prevent charge leakage from said  
58 floating gate and at a temperature below the glass transition temperature of  
59 said substrate;

60 masking off locations where MOS transistors are being formed to leave  
61 exposed only locations where EEPROM cells are being formed, and depositing a  
62 layer of metal or silicide from which the control gate of all EEPROM cells is  
63 to be formed, said deposition being by PVD, CVD, PECVD, evaporation or  
64 sputtering or some other suitable process and accomplished at a temperature  
65 below the glass transition temperature of said substrate;

66 performing the necessary photolithographic etching to define the gate  
67 islands at both said MOS transistor and EEPROM cell locations, said  
68 photolithographic etching being accomplished at temperatures below the glass  
69 transition temperature of said substrate and using chemicals and/or gases  
70 which will not attack or otherwise damage said substrate;

71 doping the source and drain regions of all said MOS transistors and  
72 EEPROM cells using the Gas Immersion Laser Doping process or any other  
73 suitable doping process which can dope said source and drain regions to  
74 suitable conductivity and which crystallizes said amorphous silicon by pulsed  
75 laser annealing and which can be accomplished at a temperature below the  
76 glass transition temperature of said substrate and using chemicals and/or  
77 gases which will not attack or otherwise damage said substrate;

78 photolithographically etching to define the lateral extents of each thin  
79 film transistor island at each MOS transistor and EEPROM cell, said  
80 photolithographic etching being accomplished at temperatures below the glass  
81 transition temperature of said substrate and using chemicals and/or gases  
82 which will not attack or otherwise damage said substrate;

83 depositing an insulation layer over all MOS transistors and EEPROM  
84 cells and etching vias therethrough for source, drain and control gate contacts

at all MOS transistor and EEPROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and EEPROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the MOS transistors and EEPROM cells together to form the desired integrated circuit functionality.

8. The process of claim 7 wherein said integrated circuit is an RFID tag transceiver, a smart card or a toy controller and further comprising the steps of etching said contact metallization conductor layer appropriately to form RF input/output terminals, and further comprising the step of printing or photolithographically forming a conductive antenna on said substrate so as to make electrical contact with said RF input/output terminals.

9. A process for manufacturing an integrated circuit including MOS transistors and ROM cells on a substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using



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chemicals which will not chemically attack or otherwise damage said substrate;

depositing a layer of amorphous silicon which is between 10 and 500 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silicon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silicon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses;

masking off areas of said integrated circuit where ROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transition temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where ROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition

(hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the ROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each ROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all ROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and ROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and ROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and ROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and ROM cells and etching vias therethrough for source, drain and control gate contacts at all MOS transistor and ROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and ROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the MOS transistors and ROM cells together to form the desired integrated circuit functionality.

10. A process for manufacturing an integrated circuit with MOS and EEPROM cells formed over an antenna on a substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will

not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

forming an antenna with one or more terminals on said layer of insulating material deposited in the previous step at a plurality of locations on said substrate by any prior art process such as silk screening or deposition and photolithographic etching accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases that will not attack or otherwise damage said substrate;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of pad contact conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors from each antenna terminal to the locations where RF input/output terminals of each corresponding integrated circuit will be formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of insulator over all MOS transistor and EEPROM cell locations and etching to form vias through said insulation layer where source and drain contacts are to be formed, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality and at a temperature below the glass transition temperature of said substrate using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line

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conductors to make all necessary source and drain connections from each MOS transistor or EEPROM cell to other devices needed to establish at least part of the connections needed for the functionality of the integrated circuit being formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silicon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silicon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses;

masking off areas of said integrated circuit where EEPROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transition temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said

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76 deposition being accomplished by PECVD at a temperature below the glass  
77 transition temperature of said substrate;

78 depositing a layer of gate conductor, typically metal or silicides by  
79 physical vapor deposition (hereafter PVD), chemical vapor deposition  
80 (hereafter CVD), PECVD, evaporation or sputtering or some other suitable  
81 process to form a control gate at the MOS transistor locations and a floating  
82 gate at the EEPROM cell locations, said deposition being accomplished at a  
83 temperature below the glass transition temperature of said substrate;

84 masking off locations where MOS transistors are being formed to leave  
85 exposed only locations where EEPROM cells are being formed, and depositing a  
86 layer of intergate insulator from which will be formed the insulation layer  
87 between the floating gate and the control gate of each EEPROM cell, said  
88 deposition being accomplished by PECVD or some other process which will  
89 form an insulator of high enough quality to prevent charge leakage from said  
90 floating gate and at a temperature below the glass transition temperature of  
91 said substrate;

92 masking off locations where MOS transistors are being formed to leave  
93 exposed only locations where EEPROM cells are being formed, and depositing a  
94 layer of metal or silicide from which the control gate of all EEPROM cells is  
95 to be formed, said deposition being by PVD, CVD, PECVD, evaporation or  
96 sputtering or some other suitable process and accomplished at a temperature  
97 below the glass transition temperature of said substrate;

98 performing the necessary photolithographic etching to define the gate  
99 islands at both said MOS transistor and EEPROM cell locations, said  
100 photolithographic etching being accomplished at temperatures below the glass  
101 transition temperature of said substrate and using chemicals and/or gases  
102 which will not attach or otherwise damage said substrate;

103 doping the source and drain regions of all said MOS transistors and  
104 EEPROM cells using the Gas Immersion Laser Doping process or any other  
105 suitable doping process which can dope said source and drain regions to  
106 suitable conductivity and which crystallizes said amorphous silicon by pulsed

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107 laser annealing and which can be accomplished at a temperature below the  
108 glass transition temperature of said substrate and using chemicals and/or  
109 gases which will not attack or otherwise damage said substrate;  
110 photolithographically etching to define the lateral extents of each thin  
111 film transistor island at each MOS transistor and EEPROM cell, said  
112 photolithographic etching being accomplished at temperatures below the glass  
113 transition temperature of said substrate and using chemicals and/or gases  
114 which will not attach or otherwise damage said substrate;  
115 depositing an insulation layer over all MOS transistors and EEPROM  
116 cells and etching vias therethrough for control gate contacts at all MOS  
117 transistor and EEPROM cell locations, said deposition being accomplished at  
118 temperatures below the glass transition temperature of said substrate and  
119 using chemicals and/or gases which will not attack or otherwise damage said  
120 substrate;  
121 depositing a layer of contact metallization conductor to fill said via  
122 holes and cover each MOS transistors and EEPROM cell location and the spaces  
123 therebetween, and photolithographically etching the conductor layer to form a  
124 contact metallization to connect all the control gates of all MOS transistors  
125 and EEPROM cells to other nodes in the circuit to form the rest of the  
126 connections necessary to form a desired integrated circuit functionality.

- 1 11. A process for manufacturing an integrated circuit with MOS and ROM cells  
2 formed over an antenna on a substrate comprising:  
3 selecting a plastic or plastic laminated to glass substrate having a large size  
4 which is compatible with the substrate size capacity of flat panel display  
5 manufacturing machines to be used to do the subsequent deposition, photolithography,  
6 etching and laser crystallization and annealing steps necessary to form said  
7 integrated circuit thereon;  
8 using flat panel display manufacturing machines to perform the following  
9 steps:

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10                    depositing a layer of insulating material which has a thickness and  
11                    Young's Modulus which are selected in light of the thickness and Young's  
12                    Modulus of said substrate so as to reduce differential strain at anticipated  
13                    operating temperatures so as to eliminate or reduce reliability problems  
14                    using processing steps performed at temperatures or in a manner which will  
15                    not exceed the glass transition temperature of said substrate and using  
16                    chemicals which will not chemically attack or otherwise damage said  
17                    substrate;

18  
19                    forming an antenna with one or more terminals on said layer of insulating  
20                    material deposited in the previous step at a plurality of locations on said substrate  
21                    by any prior art process such as silk screening or deposition and photolithographic  
22                    etching accomplished at temperatures below the glass transition temperature of said  
23                    substrate and using chemicals and/or gases that will not attack or otherwise damage  
24                    said substrate;

25  
26                    using flat panel display manufacturing machines to perform the following steps:

27                    depositing a layer of pad contact conductor such as metal or silicides  
28                    by physical vapor deposition (hereafter PVD), chemical vapor deposition  
29                    (hereafter CVD), PECVD, evaporation or sputtering or some other suitable  
30                    process and photolithographically etching to form lead line conductors from  
31                    each antenna terminal to the locations where RF input/output terminals of  
32                    each corresponding integrated circuit will be formed, said deposition being  
33                    accomplished at a temperature below the glass transition temperature of said  
34                    substrate;

35                    depositing a layer of insulator over all MOS transistor and ROM cell  
36                    locations and etching to form vias through said insulation layer where source  
37                    and drain contacts are to be formed, said deposition being accomplished by  
38                    PECVD or some other process which will form an insulator of high enough  
39                    quality and at a temperature below the glass transition temperature of said



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40 substrate using chemicals and/or gases which will not attack or otherwise  
41 damage said substrate;

42 depositing a layer of contact metallization conductor such as metal or  
43 silicides by physical vapor deposition (hereafter PVD), chemical vapor  
44 deposition (hereafter CVD), PECVD, evaporation or sputtering or some other  
45 suitable process and photolithographically etching to form lead line  
46 conductors to make all necessary source and drain connections from each MOS  
47 transistor or ROM cell to other devices needed to establish at least part of the  
48 connections needed for the functionality of the integrated circuit being  
49 formed, said deposition being accomplished at a temperature below the glass  
50 transition temperature of said substrate;

51 depositing a layer of amorphous silicon which is between 10 and  
52 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor  
53 deposition hereafter referred to as PECVD using processing steps performed  
54 at temperatures or in a manner which will not exceed the glass transition  
55 temperature of said substrate and using chemicals and/or gases which will  
56 not chemically attack or otherwise damage said substrate;

57 if higher mobilities or higher ON currents or lower threshold  
58 voltages for MOS transistors are needed for the transistors to be formed in  
59 said silicon layer than can be achieved in amorphous silicon, crystallizing said  
60 silicon layer to polycrystalline or microcrystalline form by pulse annealing  
61 the silicon layer with an excimer laser having a 308 nm wavelength using  
62 pulse durations of 30 nanoseconds or less full width at half maximum and  
63 energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses;

64 masking off areas of said integrated circuit where ROM cells, if any,  
65 are to be formed, and depositing a layer of gate insulator by PECVD at a  
66 temperature below the glass transition temperature of said substrate, said  
67 layer having a thickness suitable for thin film metal-oxide-semiconductor  
68 transistor device operation, typically between 20-500 nanometers thick;

69 masking off areas where MOS transistors are being formed to expose  
70 areas where ROM memory cells are to be formed and depositing one or more

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71 layers of gate insulator to form an insulation layer that is to lie below the  
72 floating gate, the thickness and materials selected for said one or more layers  
73 of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the  
74 floating gate from a channel region at whatever programming voltage can be  
75 achieved on said integrated circuit, said deposition being accomplished by  
76 PECVD at a temperature below the glass transition temperature of said  
77 substrate;

78 depositing a layer of gate conductor, typically metal or silicides by  
79 physical vapor deposition (hereafter PVD), chemical vapor deposition  
80 (hereafter CVD), PECVD, evaporation or sputtering or some other suitable  
81 process to form a control gate at the MOS transistor locations and a floating  
82 gate at the ROM cell locations, said deposition being accomplished at a  
83 temperature below the glass transition temperature of said substrate;

84 masking off locations where MOS transistors are being formed to leave  
85 exposed only locations where ROM cells are being formed, and depositing a  
86 layer of intergate insulator from which will be formed the insulation layer  
87 between the floating gate and the control gate of each ROM cell, said deposition  
88 being accomplished by PECVD or some other process which will form an  
89 insulator of high enough quality to prevent charge leakage from said floating  
90 gate and at a temperature below the glass transition temperature of said  
91 substrate;

92 masking off locations where MOS transistors are being formed to leave  
93 exposed only locations where ROM cells are being formed, and depositing a  
94 layer of metal or silicide from which the control gate of all ROM cells is to be  
95 formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering  
96 or some other suitable process and accomplished at a temperature below the  
97 glass transition temperature of said substrate;

98 performing the necessary photolithographic etching to define the gate  
99 islands at both said MOS transistor and ROM cell locations, said  
100 photolithographic etching being accomplished at temperatures below the glass

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101 transition temperature of said substrate and using chemicals and/or gases  
102 which will not attach or otherwise damage said substrate;  
103           doping the source and drain regions of all said MOS transistors and  
104 ROM cells using the Gas Immersion Laser Doping process or any other  
105 suitable doping process which can dope said source and drain regions to  
106 suitable conductivity and which crystallizes said amorphous silicon by pulsed  
107 laser annealing and which can be accomplished at a temperature below the  
108 glass transition temperature of said substrate and using chemicals and/or  
109 gases which will not attach or otherwise damage said substrate;  
110           photolithographically etching to define the lateral extents of each thin  
111 film transistor island at each MOS transistor and ROM cell, said  
112 photolithographic etching being accomplished at temperatures below the glass  
113 transition temperature of said substrate and using chemicals and/or gases  
114 which will not attach or otherwise damage said substrate;  
115           depositing an insulation layer over all MOS transistors and ROM cells  
116 and etching vias therethrough for control gate contacts at all MOS transistor  
117 and ROM cell locations, said deposition being accomplished at temperatures  
118 below the glass transition temperature of said substrate and using chemicals  
119 and/or gases which will not attach or otherwise damage said substrate;  
120           depositing a layer of contact metallization conductor to fill said via  
121 holes and cover each MOS transistors and ROM cell location and the spaces  
122 therebetween, and photolithographically etching the conductor layer to form a  
123 contact metallization to connect all the control gates of all MOS transistors  
124 and ROM cells to other nodes in the circuit to form the rest of the connections  
125 necessary to form a desired integrated circuit functionality.

- 192           12. A process of making a large number of integrated EEPROM or ROM or static RAM  
193 cells on a large substrate comprising:  
194           selecting a glass substrate having a large size which is compatible with the  
195 substrate size capacity of flat panel display manufacturing machines to be used to do

196 the subsequent deposition, photolithography, etching and laser crystallization and  
197 annealing steps necessary to form said EEPROM or ROM or static RAM cells thereon;  
198 using flat panel display manufacturing machines to do the insulation, metal  
199 and semiconductor deposition steps, and the photolithography, etching and pulsed  
200 laser crystallization and annealing steps necessary to form a plurality of EEPROM or  
201 ROM or static RAM memory cells directly on said glass substrate, all said processing  
202 steps performed at temperatures or in a manner which will not exceed the glass  
203 transition temperature of said substrate and using chemicals which will not  
204 chemically attack or otherwise damage said substrate.

1 13. A process for manufacturing an integrated circuit including MOS transistors and  
2 EEPROM cells on a substrate comprising:

3 selecting a glass substrate having a large size which is compatible with the  
4 substrate size capacity of flat panel display manufacturing machines to be used to do  
5 the subsequent deposition, photolithography, etching and laser crystallization and  
6 annealing steps necessary to form said integrated circuit thereon;

7 using flat panel display manufacturing machines to perform the following  
8 steps:

9 depositing a layer of insulating material using processing steps  
10 performed at temperatures or in a manner which will not exceed the glass  
11 transition temperature of said substrate and using chemicals which will not  
12 chemically attack or otherwise damage said substrate;

13 depositing a layer of amorphous silicon which is between 10 and  
14 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor  
15 deposition hereafter referred to as PECVD using processing steps performed  
16 at temperatures or in a manner which will not exceed the glass transition  
17 temperature of said substrate and using chemicals and/or gases which will  
18 not chemically attack or otherwise damage said substrate;

19 if higher mobilities or higher ON currents or lower threshold  
20 voltages for MOS transistors are needed for the transistors to be formed in  
21 said silicon layer than can be achieved in amorphous silicon, crystallizing said

silicon layer to polycrystalline or microcrystalline form by pulse annealing the silicon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses; masking off areas of said integrated circuit where EEPROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transition temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick; masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate; depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the EEPROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate; masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each EEPROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said

floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all EEPROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and EEPROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and EEPROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and EEPROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and EEPROM cells and etching vias therethrough for source, drain and control gate contacts at all MOS transistor and EEPROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

83                    depositing a layer of contact metallization conductor to fill said via  
84                    holes and cover each MOS transistors and EEPROM cell location and the spaces  
85                    therebetween, and photolithographically etching the conductor layer to form a  
86                    contact metallization to connect all the MOS transistors and EEPROM cells  
87                    together to form the desired integrated circuit functionality.

1                    14. A process for manufacturing an integrated circuit including MOS transistors and  
2                    ROM cells on a substrate comprising:

3                    selecting a glass substrate having a large size which is compatible with the  
4                    substrate size capacity of flat panel display manufacturing machines to be used to do  
5                    the subsequent deposition, photolithography, etching and laser crystallization and  
6                    annealing steps necessary to form said integrated circuit thereon;

7                    using flat panel display manufacturing machines to perform the following  
8                    steps:

9                    depositing a layer of insulating material using processing steps  
10                    performed at temperatures or in a manner which will not exceed the glass  
11                    transition temperature of said substrate and using chemicals which will not  
12                    chemically attack or otherwise damage said substrate;

13                    depositing a layer of amorphous silicon which is between 10 and 500  
14                    nanometers thick by sputtering or by plasma enhanced chemical vapor  
15                    deposition hereafter referred to as PECVD using processing steps performed  
16                    at temperatures or in a manner which will not exceed the glass transition  
17                    temperature of said substrate and using chemicals and/or gases which will  
18                    not chemically attack or otherwise damage said substrate;

19                    if higher mobilities or higher ON currents or lower threshold  
20                    voltages for MOS transistors are needed for the transistors to be formed in  
21                    said silicon layer than can be achieved in amorphous silicon, crystallizing said  
22                    silicon layer to polycrystalline or microcrystalline form by pulse annealing  
23                    the silicon layer with an excimer laser having a 308 nm wavelength using  
24                    pulse durations of 30 nanoseconds or less full width at half maximum and  
25                    energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses;

26                   masking off areas of said integrated circuit where ROM cells, if any,  
27                   are to be formed, and depositing a layer of gate insulator by PECVD at a  
28                   temperature below the glass transition temperature of said substrate, said  
29                   layer having a thickness suitable for thin film metal-oxide-semiconductor  
30                   transistor device operation, typically between 20-500 nanometers thick;

31                   masking off areas where MOS transistors are being formed to expose  
32                   areas where ROM memory cells are to be formed and depositing one or more  
33                   layers of gate insulator to form an insulation layer that is to lie below the  
34                   floating gate, the thickness and materials selected for said one or more layers  
35                   of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the  
36                   floating gate from a channel region at whatever programming voltage can be  
37                   achieved on said integrated circuit, said deposition being accomplished by  
38                   PECVD at a temperature below the glass transition temperature of said  
39                   substrate;

40                   depositing a layer of gate conductor, typically metal or silicides by  
41                   physical vapor deposition (hereafter PVD), chemical vapor deposition  
42                   (hereafter CVD), PECVD, evaporation or sputtering or some other suitable  
43                   process to form a control gate at the MOS transistor locations and a floating  
44                   gate at the ROM cell locations, said deposition being accomplished at a  
45                   temperature below the glass transition temperature of said substrate;

46                   masking off locations where MOS transistors are being formed to leave  
47                   exposed only locations where ROM cells are being formed, and depositing a  
48                   layer of intergate insulator from which will be formed the insulation layer  
49                   between the floating gate and the control gate of each ROM cell, said deposition  
50                   being accomplished by PECVD or some other process which will form an  
51                   insulator of high enough quality to prevent charge leakage from said floating  
52                   gate and at a temperature below the glass transition temperature of said  
53                   substrate;

54                   masking off locations where MOS transistors are being formed to leave  
55                   exposed only locations where ROM cells are being formed, and depositing a  
56                   layer of metal or silicide from which the control gate of all ROM cells is to be



formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and ROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and ROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and ROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and ROM cells and etching vias therethrough for source, drain and control gate contacts at all MOS transistor and ROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and ROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the MOS transistors and ROM cells together to form the desired integrated circuit functionality.

1           15. A process for manufacturing an integrated circuit with MOS and EEPROM cells  
2 formed over an antenna on a substrate comprising:

3           selecting a glass substrate having a large size which is compatible with the  
4 substrate size capacity of flat panel display manufacturing machines to be used to do  
5 the subsequent deposition, photolithography, etching and laser crystallization and  
6 annealing steps necessary to form said integrated circuit thereon;

7           using flat panel display manufacturing machines to perform the following  
8 steps:

9           depositing a layer of insulating material using processing steps  
10 performed at temperatures or in a manner which will not exceed the glass  
11 transition temperature of said substrate and using chemicals which will not  
12 chemically attack or otherwise damage said substrate;

13  
14           forming an antenna with one or more terminals on said layer of insulating  
15 material deposited in the previous step at a plurality of locations on said substrate  
16 by any prior art process such as silk screening or deposition and photolithographic  
17 etching accomplished at temperatures below the glass transition temperature of said  
18 substrate and using chemicals and/or gases that will not attack or otherwise damage  
19 said substrate;

20  
21           using flat panel display manufacturing machines to perform the following steps:

22           depositing a layer of pad contact conductor such as metal or silicides  
23 by physical vapor deposition (hereafter PVD), chemical vapor deposition  
24 (hereafter CVD), PECVD, evaporation or sputtering or some other suitable  
25 process and photolithographically etching to form lead line conductors from  
26 each antenna terminal to the locations where RF input/output terminals of  
27 each corresponding integrated circuit will be formed, said deposition being  
28 accomplished at a temperature below the glass transition temperature of said  
29 substrate;

30 depositing a layer of insulator over all MOS transistor and EEPROM  
31 cell locations and etching to form vias through said insulation layer where  
32 source and drain contacts are to be formed, said deposition being accomplished  
33 by PECVD or some other process which will form an insulator of high enough  
34 quality and at a temperature below the glass transition temperature of said  
35 substrate using chemicals and/or gases which will not attack or otherwise  
36 damage said substrate;

37 depositing a layer of contact metallization conductor such as metal or  
38 silicides by physical vapor deposition (hereafter PVD), chemical vapor  
39 deposition (hereafter CVD), PECVD, evaporation or sputtering or some other  
40 suitable process and photolithographically etching to form lead line  
41 conductors to make all necessary source and drain connections from each MOS  
42 transistor or EEPROM cell to other devices needed to establish at least part of  
43 the connections needed for the functionality of the integrated circuit being  
44 formed, said deposition being accomplished at a temperature below the glass  
45 transition temperature of said substrate;

46 depositing a layer of amorphous silicon which is between 10 and  
47 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor  
48 deposition hereafter referred to as PECVD using processing steps performed  
49 at temperatures or in a manner which will not exceed the glass transition  
50 temperature of said substrate and using chemicals and/or gases which will  
51 not chemically attack or otherwise damage said substrate;

52 if higher mobilities or higher ON currents or lower threshold  
53 voltages for MOS transistors are needed for the transistors to be formed in  
54 said silicon layer than can be achieved in amorphous silicon, crystallizing said  
55 silicon layer to polycrystalline or microcrystalline form by pulse annealing  
56 the silicon layer with an excimer laser having a 308 nm wavelength using  
57 pulse durations of 30 nanoseconds or less full width at half maximum and  
58 energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses;

59 masking off areas of said integrated circuit where EEPROM cells, if  
60 any, are to be formed, and depositing a layer of gate insulator by PECVD at a

temperature below the glass transition temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the EEPROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each EEPROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all EEPROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or

sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and EEPROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and EEPROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and EEPROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and EEPROM cells and etching vias therethrough for control gate contacts at all MOS transistor and EEPROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and EEPROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the control gates of all MOS transistors and EEPROM cells to other nodes in the circuit to form the rest of the connections necessary to form a desired integrated circuit functionality.

1           16. A process for manufacturing an integrated circuit with MOS and ROM cells  
2      formed over an antenna on a substrate comprising:  
3           selecting a glass substrate having a large size which is compatible with the  
4      substrate size capacity of flat panel display manufacturing machines to be used to do  
5      the subsequent deposition, photolithography, etching and laser crystallization and  
6      annealing steps necessary to form said integrated circuit thereon;  
7           using flat panel display manufacturing machines to perform the following  
8      steps:  
9           depositing a layer of insulating material which has a thickness and  
10     Young's Modulus which are selected in light of the thickness and Young's  
11     Modulus of said substrate so as to reduce differential strain at anticipated  
12     operating temperatures so as to eliminate or reduce reliability problems  
13     using processing steps performed at temperatures or in a manner which will  
14     not exceed the glass transition temperature of said substrate and using  
15     chemicals which will not chemically attack or otherwise damage said  
16     substrate;  
17  
18     forming an antenna with one or more terminals on said layer of insulating  
19     material deposited in the previous step at a plurality of locations on said substrate  
20     by any prior art process such as silk screening or deposition and photolithographic  
21     etching accomplished at temperatures below the glass transition temperature of said  
22     substrate and using chemicals and/or gases that will not attack or otherwise damage  
23     said substrate;  
24  
25     using flat panel display manufacturing machines to perform the following steps:  
26           depositing a layer of pad contact conductor such as metal or silicides  
27     by physical vapor deposition (hereafter PVD), chemical vapor deposition  
28     (hereafter CVD), PECVD, evaporation or sputtering or some other suitable  
29     process and photolithographically etching to form lead line conductors from  
30     each antenna terminal to the locations where RF input/output terminals of

each corresponding integrated circuit will be formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of insulator over all MOS transistor and ROM cell locations and etching to form vias through said insulation layer where source and drain contacts are to be formed, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality and at a temperature below the glass transition temperature of said substrate using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors to make all necessary source and drain connections from each MOS transistor or ROM cell to other devices needed to establish at least part of the connections needed for the functionality of the integrated circuit being formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silicon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silicon layer with an excimer laser having a 308 nm wavelength using

pulse durations of 30 nanoseconds or less full width at half maximum and  
 energy density between 30-600 mJ/cm<sup>2</sup> per pulse using one or more pulses;  
 masking off areas of said integrated circuit where ROM cells, if any,  
 are to be formed, and depositing a layer of gate insulator by PECVD at a  
 temperature below the glass transition temperature of said substrate, said  
 layer having a thickness suitable for thin film metal-oxide-semiconductor  
 transistor device operation, typically between 20-500 nanometers thick;  
 masking off areas where MOS transistors are being formed to expose  
 areas where ROM memory cells are to be formed and depositing one or more  
 layers of gate insulator to form an insulation layer that is to lie below the  
 floating gate, the thickness and materials selected for said one or more layers  
 of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the  
 floating gate from a channel region at whatever programming voltage can be  
 achieved on said integrated circuit, said deposition being accomplished by  
 PECVD at a temperature below the glass transition temperature of said  
 substrate;  
 depositing a layer of gate conductor, typically metal or silicides by  
 physical vapor deposition (hereafter PVD), chemical vapor deposition  
 (hereafter CVD), PECVD, evaporation or sputtering or some other suitable  
 process to form a control gate at the MOS transistor locations and a floating  
 gate at the ROM cell locations, said deposition being accomplished at a  
 temperature below the glass transition temperature of said substrate;  
 masking off locations where MOS transistors are being formed to leave  
 exposed only locations where ROM cells are being formed, and depositing a  
 layer of intergate insulator from which will be formed the insulation layer  
 between the floating gate and the control gate of each ROM cell, said deposition  
 being accomplished by PECVD or some other process which will form an  
 insulator of high enough quality to prevent charge leakage from said floating  
 gate and at a temperature below the glass transition temperature of said  
 substrate;



masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all ROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and ROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and ROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and ROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and ROM cells and etching vias therethrough for control gate contacts at all MOS transistor and ROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and ROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a

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122 contact metallization to connect all the control gates of all MOS transistors  
123 and ROM cells to other nodes in the circuit to form the rest of the connections  
124 necessary to form a desired integrated circuit functionality.  
125  
126

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